**In The Claims:**

Please amend the claims as follows:

Claim 1. (currently amended) A motherboard with reduced power consumption, comprising:

a memory module slot for ~~connecting~~ receiving a memory module therein;

a DDR (Double data rate) termination array, coupled [[~~to~~]] between the memory module slot and a voltage source, ~~for providing~~ comprising a plurality of termination resistors connected ~~between~~ to [[a]] the voltage source and a plurality of switches between the plurality of termination resistors and the memory module slot, wherein the plurality of switches controlling connections between the ~~voltage source~~ memory module slot and the termination resistors are controlled according to ~~an indication of~~ a control signal; and

a controller chip set, coupled to the memory module slot and the DDR termination array ~~to provide~~, providing the control signal, wherein when the motherboard enters a power saving mode, or before the memory module is inserted into the memory module slot, the control signal ~~commands the DDR termination array to cut~~ cuts off the connections between the termination resistors and the voltage source; and wherein in connection, the plurality of termination resistors are coupled to the memory module in the memory module slot through the plurality of switches.

2. (original) The motherboard according to claim 1, wherein the control signal includes a clock enable signal.

3. (original) The motherboard according to claim 1, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).

4. (original) The motherboard according to claim 1, wherein the motherboard is used in a laptop computer.

5. (original) The motherboard according to claim 1, wherein the controller chip set comprises a north bridge chip.

6. (currently amended) The motherboard according to claim 1, wherein the DDR termination array further comprises:

a plurality of signal terminals, coupled ~~to a plurality of corresponding signal buses~~ between the memory module slot and the plurality of switches.[[;]]

~~a plurality of switches, wherein each of the switches comprises a first terminal, a second terminal and a control terminal, and each of the first terminals is connected to one of the signal terminals; and~~

~~wherein the control signal commands the switches being switched on or off for controlling the connections between the termination resistors and the voltage source.~~

**Claim 7. (canceled)**

8. (currently amended) A motherboard with reduced power consumption, comprising:

a memory module slot for ~~connecting~~ receiving a memory module;

a plurality of termination resistors, ~~each of the termination resistors comprises a first terminal and a second terminal, wherein the first terminals of the termination resistors are~~ coupled to the memory module slot;

a switch, coupled between the plurality of termination resistors and a voltage source, on/off of the switch being controlled by a control signal ~~comprising a first terminal, a second~~

~~terminal and a control terminal, wherein the second terminals of the termination resistors are coupled to the first terminal of the switch, the second terminal of the switch is coupled to a voltage source, and the control terminal is used to receive a control signal~~; and

a controller chip set, coupled to the memory module slot and the switch to provide the control signal, wherein when the motherboard enters a power saving mode or when the memory module is not inserted in the memory module slot, the control signal commands the switch to cut off the connection between the termination resistors and the voltage source; and wherein in connection, the plurality of termination resistors are coupled to the memory module in the memory module slot.

9. (original) The motherboard according to claim 8, wherein the control signal comprises a clock enable signal.

10. (original) The motherboard according to claim 8, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).

11. (original) The motherboard according to claim 8, wherein the motherboard is used in a laptop computer.

12. (original) The motherboard according to claim 8, wherein the controller chip set comprises a north bridge chip.

13. (currently amended) An operation method of a motherboard with reduced power consumption, wherein the motherboard comprises a memory module slot for receiving a memory module and a plurality of termination resistors, the termination resistors~~, the memory module slot~~ and a voltage source form an operation circuit, the operation method comprising:

~~providing a control signal wherein a connection between the voltage source and the operation circuit is controlled by an indication of the control signal;~~

using [[~~the~~]] a control signal to cut off [[~~the~~]] a connection between the ~~voltage source~~ memory module and the operation circuit when the motherboard enters a power saving mode or when the memory module slot is not inserted with [[~~a~~]] the memory module; and

using the control signal to establish the connection between the ~~voltage source~~ memory module slot and the operation circuit when the motherboard enters a normal operation mode and when the memory module slot is inserted with the memory module.

14. (original) The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the memory module slot.

15. (original) The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the voltage source.

16. (currently amended) The operation method according to claim 13, wherein the control signal is [[~~an~~]] a clock enable signal provided by a laptop computer.